

APPLICATION FOR  
UNITED STATES LETTERS PATENT

FOR

AN AVERAGE CURRENT ESTIMATION SCHEME  
FOR SWITCHING MODE POWER SUPPLIES

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1                   **AN AVERAGE CURRENT ESTIMATION SCHEME**  
2                   **FOR SWITCHING MODE POWER SUPPLIES**

3  
4                   **RELATED APPLICATIONS**

5  
6           The present invention is based on Provisional Serial No. 60/334,849 filed on  
7   October 31, 2001. The content of this application is incorporated herein by reference.  
8

9                   **FIELD OF THE INVENTION**

10  
11           This invention relates to switching mode power supplies (SMPS) and their control  
12   and in particular to a means of accurately measuring the output current being delivered to  
13   a load. The power supply has a dc current estimation circuit that extracts dc current  
14   information from a measured peak current signal.  
15

16                   **BACKGROUND OF THE INVENTION**

17  
18           In a dc/dc converter, the output current is often needed in many applications, such  
19   as current sharing control, current monitoring, etc. The most frequently used method of  
20   obtaining dc output current is to use a current sensing resistor, or current shunt, at the  
21   output of the dc/dc converter. The problems associated with the current shunt are two  
22   fold. First, a current shunt in the output current path will generate a significant power  
23   loss, especially for low output voltage dc/dc converters. Second, to extract usable  
24   information from the sensed current signal from a noisy environment, a differential  
25   amplifier is often needed to pick up the signal and convert it to a proper level, thus  
26   increasing the circuit complexity. Therefore, what is needed in the art is a low loss and  
27   simple method of estimating dc output current for a dc/dc converter.

28           **FIG. 1** illustrates a prior art circuit that can be used to obtain the dc output current  
29   by sensing the switch current, through either a current shunt or a current sensing  
30   transformer. U. S. Patent No. 5,457,620 to Dromgoole provides a general explanation of  
31   this circuit. An input voltage **102** is supplied to the power transformer **106**. The power

1 transformer 106 has a primary winding 108 and a secondary winding 110. The sensed  
2 current signal, which is the voltage 123 across the current shunt 124 is supplied to a load  
3 switch 126 in series with a low pass filter made of a resistor 128 and a capacitor 130.  
4 The switch 126 is controlled by the same signal driving the power stage switch 122.  
5 When the current signal is sensed by the current shunt or the current sensing transformer,  
6 the switch is on and the sensed current signal is let through the low pass filter. The low  
7 pass filter helps convert that pulsed signal into the dc current signal. When the power  
8 stage switch is off and the current signal is zero, the switch is turned off and the low pass  
9 filter holds the sensed current signal till next switch cycle commences.

10 Although this is a very simple dc current estimation circuit and works reasonably  
11 well for many applications, it does have its drawback. The control switch is a floating  
12 drive, i.e., the control voltage is not referenced to the gate and the source if a MOSFET is  
13 used to implement the current estimation switch. The drive signal becomes part of the  
14 current sensing signal, introducing extra error in the estimated current signal. To  
15 eliminate the error, some kind of floating drive circuit is needed, either a gate drive  
16 transformer or a high side driver, which will in turn complicate the overall circuit.  
17

## SUMMARY OF THE INVENTION

The present invention relates to a switching mode power supply and more specifically to an average current estimation circuit that can be used to provide a signal that is proportional to the output current based on a sensed peak current signal by using either a current shunt or a current sensing transformer. In each embodiment, there is a diode through which the peak current signal is fed to a control switch in series with a resistor. A RC filter is in parallel with the series combination of the switch and the resistor.

Compared with the prior art, the invention offers several extra benefits in addition to provide a dc current signal from a sensed peak current. First, a control switch is referenced to the ground, and therefore provides better current estimation accuracy. No extra error is introduced even without the use of a floating drive as shown in the prior art. Next, the peak current signal is always available regardless of the status of the control switch. By separating the peak and average current signals, the converter can be better controlled and both peak current mode control and current sharing control can be optimized. Last, referencing the peak current and average current signals to the different grounds provides freedom to implement different control schemes.

1                   **BRIEF DESCRIPTION OF THE DRAWINGS**

2           The novel features believed characteristic of the invention are set forth in the  
3   appended claims. The invention itself however, as well as a preferred mode of use,  
4   further objects and advantages thereof, will best be understood by reference to the  
5   following detailed description of an illustrative embodiment when read in conjunction  
6   with the accompanying drawings, wherein:

7           **FIG. 1** is a schematic of a prior art of the average current estimation circuit for a  
8   switch mode power supply using Dromgools patent ;

9           **FIG. 2** shows the basic circuit that estimates dc output current through sensing the  
10   power stage switch current;

11          **FIG. 3** illustrates the dc output current estimation circuit when using a current  
12   shunt to sense the switch current;

13          **FIGS. 4 and 5** illustrate the dc output current estimation circuit when using a  
14   current sensing transformer to sense the switch current;

15          **FIG. 6** shows the dc output current estimation circuit when peak current signal  
16   and average current signal are referenced to different grounds; and

17          **FIG. 7** illustrates the use of an op-amp and diode circuit for temperature  
18   compensation for the sensed dc current signal.  
19

## DETAILED DESCRIPTION OF THE DRAWINGS

**FIG. 2** illustrates a basic circuit **200** that estimates dc output current through sensing the power stage switch current. The basic circuit consists of a diode **204**, a resistor **206** in series with a switch **208**, another resistor **210** and a capacitor **212**. When the sensed peak current **202** is applied to the circuit, the switch **208** turns on. The voltage across the resistor **206** and switch **208**, designated  $V_S$ , is the sensed peak current  $V_{IpK}$  less a forward diode voltage drop. Resistor **210** and capacitor **212** form a low pass filter which filters out the voltage ripple of  $V_S$  and generates a smooth dc voltage **213** whose value corresponds to the output dc current and is independent of the input voltage provided the magnetizing current of the power transformer is neglected. The diode **204** lets the sensed switch current signal through but prevents the voltage  $V_S$  as well as  $V_{Iavg}$  from being discharged. The switch **208** is a control switch to adjust the sensed dc current signal to reflect the real dc output current. If the load current is decreased, for example, the in-coming current sensing signal is lower than the sensed dc current signal  $V_{Iavg}$ . As a result,  $V_{Iavg}$  will be discharged during turn-on of switch **208** through resistors **210** and **206**, and switch **208**, being brought down to the level corresponding to the level of the new dc output current.

For this basic implementation and other circuits described below, a timing diagram is also provided showing the voltage waveforms at different points in the circuit. For example, timing diagram **250** shows the sensed peak current signal that is a pulsed voltage  $V_{IpK}$ . **202**. Switch **208** has a duty cycle as shown by waveform **220**. The voltage across switch **208** and resistor **206**,  $V_S$ , is shown by waveform **222**. And  $V_{Iavg}$ , the dc voltage signal that is indicative of the output current seen by the load, is shown with waveform **224**. Waveforms **202**, **220**, **222**, and **224** are identical for all embodiments. Further, in each embodiment, the basic circuit **200** will be outlined.

With the basic estimation circuit defined, we can apply this circuit to various topologies to implement dc output current estimation. The first circuit discussed here is a forward converter **300** using a resistor to sense the primary switch current  $I$  **302**, as shown in **FIG. 3**. The average current sensing circuit **200** is directly connected to the current sensing resistor **304**. During on time of the primary switch **306** the primary

switch current  $I$  is the reflected secondary output inductor current  $I_{L1}$ . The current generates a voltage signal  $V_{ipk}$  across the current shunt resistor **304**, which is fed to the average current estimation circuit **200**. At the junction of diode **204**, resistor **210**, and resistor **206** a dc signal  $V_S$  is obtained which has a small ripple superimposed onto. This ripple is shown in the timing diagram with waveform **320**. Note that switch **208** is synchronized with switch **306**. After the low pass filter, a smooth voltage  $V_{lavg}$  is obtained across the capacitor **212**.

Now turn attention to the same forward circuit **400** with a current sensing transformer **402** as shown in **FIG. 4**. Since it is identical to that given in **FIG. 3**, the power stage is not shown in **FIG. 4**. Now the primary switch current  $I$  **404**, which is the reflected output inductor current  $I_{L1}$  during the on time, flows through the current sensing transformer **402**. This current is reflected on the secondary side of the current sensing transformer, part of which flows through diode **406** generating the sensed switch current signal across the burden resistor **408** while the rest of which flows through diode **410** generating  $V_S$ . Assuming the same voltage drop on the diodes **406** and **410**,  $V_S$  is equal to  $V_{ipk}$ . Again the sensed signal  $V_S$  is filtered by the low pass filter, generating a smooth dc current signal  $V_{lavg}$ . Examining the circuit given in **FIG. 4** carefully, it can be seen that the circuit branches containing diode **406** and diode **410** form a current divider, thus the final sensed signals depend on the resistor values of **408**, **412**, **414**, and  $V_{CR10}$  and  $V_{CR11}$ . To simplify circuit design while maintaining one-to-one mapping relationships between the switch current and the sensed  $V_{ipk}$  as well as between the dc output current and sensed  $V_{lavg}$ , the circuit can be designed such that the values of resistor **412** > resistor **414** >> resistor **408**. The peak current sensing and dc output current sensing are no longer coupled by separating the resistor values this way. In addition, one can choose diode **406** and diode **410** being the same type diode, better yet physically in the same package, and thus the forward voltage drop variations caused by temperature change will increase or decrease in the same direction, thereby eliminating the temperature effect.

**FIG. 5** shows another embodiment of the average current estimation circuit **500** when a current sensing transformer **502** is used. Now the average current estimation circuit is connected to the burden resistor **504**, and the  $V_{ipk}$  signal is directly fed to the diode **512** yielding a dc output current signal. The control of the switch **514** is identical to

1 that in **FIG. 4**, and the result is the same except that  $V_S$  is one diode voltage drop lower  
2 than  $V_{IpK}$  signal.

3 In some applications, the sensed dc output current and the peak switch current are  
4 referenced to different grounds. A dc/dc converter where peak current protection is  
5 implemented on the primary side while the current share control is implemented on the  
6 secondary side is a typical example. **FIG. 6** shows the embodiment of this concept. To  
7 simplify the drawing, again, the power stage is omitted. Notice the difference of the  
8 current sensing transformer **602** from the previous embodiments. The current sensing  
9 transformer has two secondary windings, **606** and **608**, one feeding diode **610** to provide  
10 a sensed peak current signal, one feeding diode **612** to provide a sensed dc output current  
11 signal. Since the current sensing transformer **602** has two secondary sides, the two  
12 signals can be referenced to different grounds SGND1 and SGND2. Selection of the  
13 circuit parameters such as resistor values can follow the guidelines described above. One  
14 can even design the current sensing transformer secondary windings differently so that  
15 the peak current signal and the average dc current signal can be flexibly scaled to the  
16 levels desired.

17 **FIG. 7** shows an improvement of the embodiment presented in **FIG. 5** where the  
18 sensed dc average current  $V_{Ivg}$  is one diode voltage drop below the incoming signal  $V_{IpK}$ .  
19 Adding an op-amp **702** after the low pass filter provides a possibility to recover this  
20 voltage drop. A diode **704** is between the output and the negative input of the op-amp. By  
21 choosing the resistor **705** value to be equal to the resistor **714**, the output of op-amp **702**  
22 generates a signal  $V_{Iavg}$  which excludes the voltage drop of diode **706**.

23 In summary, the present invention provides several benefits in addition to  
24 providing a dc current from a sensed peak current. First, the control switch is referenced  
25 to the ground, and therefore floating drive for the series switch in the prior art **FIG. 1** is  
26 not necessary. Second, the peak current signal is always available regardless of the  
27 status of the control switch. By separating the peak and average current signals, the  
28 converter can be better controlled and both peak current mode control and current sharing  
29 control can be optimized. Third, referencing the peak current and average current signals  
30 to the different grounds provides freedom to implement different control schemes.



1 In the above embodiments, the control switch (e.g., 208 in Fig. 2) is synchronized  
2 with the in-coming peak current signal  $V_{Ip}$ , i.e., the switch is on when the peak current  
3 signal is applied to the current estimation circuit and the switch is off when the peak  
4 current is zero. It should be pointed out that the control signal for the switch in the  
5 average current estimation circuit can be implemented in different ways, such as  
6 inverting, AND, OR or other operations of the power switch(es) control signal(s)  
7 depending on how the current sensing is implemented and the topology used.

8 Although the present invention has been described in detail, those skilled in the  
9 art should understand that they can make various changes, substitutions and alterations  
10 herein without departing from the spirit and scope of the invention in its broadest form.  
11 Indeed, the term “switch mode power supply” is meant to include all topologies with or  
12 without transformer isolation. Examples of such variations are implementations of the  
13 proposed current sensing scheme to different topologies, such as buck, full bridge, half  
14 bridge, or push-pull. A MOSFET is used as the control switch in the above  
15 embodiments, other types of active switch such as a bipolar junction transistor is also a  
16 viable choice. Slight modification such as exchanging the position of the control switch  
17 **Q10** and the resistor **R12** does not change the nature of the circuit and operation  
18 principle.